We claim:

1. An electronic component, comprising:

at least one semiconductor chip, the semiconductor chip including an active chip top side, a chip rear side and a plurality of contact areas arranged on the chip top side;

a circuit carrier, the circuit carrier having a carrier top side;

at least one patterned rewiring layer the rewiring layer having external contact areas;

a plurality of external contacts arranged on the external contact areas;

wherein the chip rear side is arranged on the carrier top side,

the rewiring layer extends over the active chip top side and over the carrier top side, and

the external contacts have heights, the heights being adapted to the level difference between chip top side and carrier top side, the chip top side having a first external contact top side, the carrier top side having a second external contact top side, the external contact top sides being disposed at a common level.

2. The electronic component according to claim 1, wherein the circuit carrier has materials, the materials having thermal expansion coefficients adapted to the thermal expansion coefficient of a circuit substrate of a superordinate circuit.

3. The electronic component according to claim 1, wherein the circuit carrier has metal.

4. The electronic component according to claim 1, wherein an elastic adhesive layer is arranged between the chip rear side of the semiconductor chip and the carrier top side.

5. The electronic component according to claim 1, wherein the circuit carrier has the form of a wafer on which the semiconductor chips are arranged in rows and columns at component positions.

6. Electronic component according to claim 1, wherein at least the external contacts on the semiconductor chip have conduction paths on a compliant bump.

7. A system, comprising:

a circuit carrier, the circuit carrier being made of metal and a plurality of semiconductor chips, the semiconductor chips having chip top sides and chip rear sides, the semiconductor chips being arranged with the chip rear side on a respective carrier top side, the semiconductor chips being electrically connected via a common rewiring layer among one another and to external contacts having different heights, the different heights of the external contacts levelling the level differences between the chip top sides and the carrier top side such that external contact top sides are disposed at a common level.

8. The circuit module according to claim 7, wherein the plurality of semiconductor chips are stacked one on the other, rewiring layers are arranged between the stacked semiconductor chips rewiring layers insulated conductor tracks lead to the external contacts on the circuit carrier at least the topmost semiconductor chip of the semiconductor chip stack having compliant, rubber-elastic external contacts.

9. A method for producing electronic components, comprising:

producing a wafer-type or rectangular circuit carrier, the circuit being made of metal with component positions arranged in rows and columns on a carrier top side;

applying a first insulation layer;

applying semiconductor chips in the component positions;

applying a rubber-elastic material on the edge sides of the semiconductor chip, the rubber-elastic material being a transition between the chip top side and the circuit carrier top side covered with an insulation layer, with simultaneous formation of rubber-elastic external contact bodies for compliant external contacts;

applying a rewiring layer with formation of conduction paths from top sides of the compliant external contacts to contact areas of the semiconductor chip and with formation of rewiring lines from contact areas of the semiconductor chip to external contact areas on that surface of the circuit carrier with insulation layer which is not covered by the semiconductor chip;

applying outer external contacts having a different height with respect to a height of external contacts on the semiconductor chip as level equalization between chip top sides and carrier surface such that external contact top sides form a common level; and

dividing the circuit carrier into individual components at the component positions.

10. The method according to claim 9, wherein the semiconductor chips are adhesively bonded by chip rear sides onto the carrier top side with formation of an adhesive meniscus at edge sides of the semiconductor chips by an elastic adhesive.

11. The method according to claim 9, wherein applying the rewiring layer includes:

applying an insulation layer the insulation layer partially covering the active chip top sides and the remaining carrier top side;

printing a buffer layer made of rubber-elastic material for fluid transitions from the level of the carrier top side to the level of the chip top side and simultaneous printing application of contact bodies in the form of compliant bumps at least on the chip tops sides made of rubber-elastic material,

applying a closed metal layer to the three-dimensionally patterned surfaces with formation of passage contacts in passage openings to the contact areas of the semiconductor chip;

patterning the closed metal layer to form a rewiring layer, the external contact areas and rewiring lines between passage contacts among one another and from passage contacts to external contact areas and conduction paths between external contact top sides on the bumps and contact areas on the semiconductor chip; and

applying a refinement layer to topmost external contact areas.

12. The method according to claim 9, wherein

a first rewiring layer with buried rewiring lines to external contact areas on the circuit carrier is applied on a first semiconductor chip; and

at least one further topmost semiconductor chip with compliant external contacts is applied to the first rewiring layer.

13. The electronic component according to claim 4, wherein the elastic adhesive layer is conductive.

14. A system, comprising:

a circuit carrier, the circuit carrier being made of metal and a plurality of semiconductor chips, the semiconductor chips having chip top sides and chip rear sides, the semiconductor chips being arranged with the chip rear side on a semiconductor chip, the semiconductor chips being electrically connected via a common rewiring layer among one another and to external contacts having different heights, the different heights of the external contacts levelling the level differences between the chip top sides and the carrier top side such that external contact top sides are disposed at a common level.

15. The circuit module according to claim 14, wherein the plurality of semiconductor chips are stacked one on the other, rewiring layers are arranged between the stacked semiconductor chips rewiring layers insulated conductor tracks lead to the external contacts on the circuit carrier at least the topmost semiconductor chip of the semiconductor chip stack having compliant, rubber-elastic external contacts.

16. The method according to claim 9, wherein the first insulation layer is a patterned insulation layer.

17. The method according to claim 10, wherein the elastic adhesive is electrically conductive.